

Figure 1

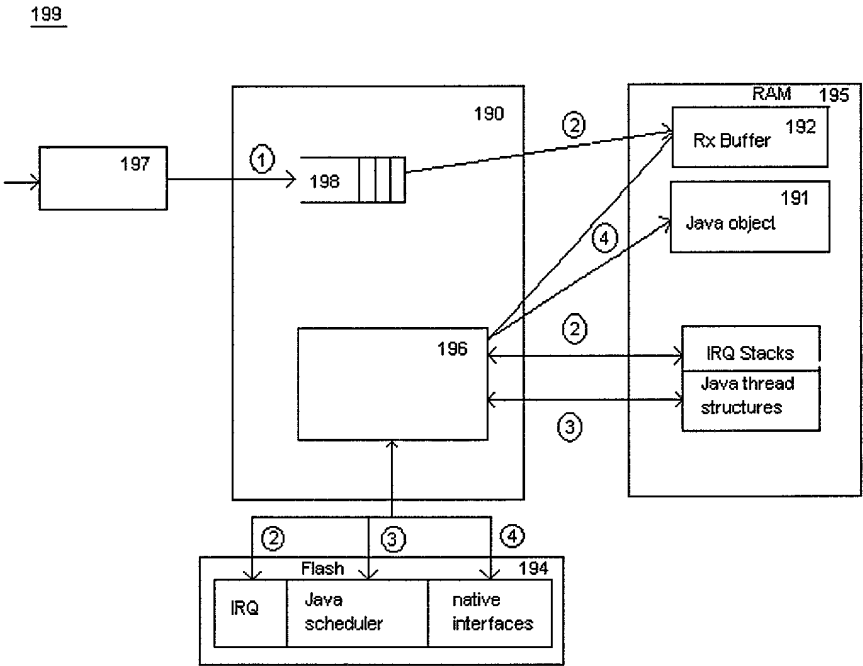


Figure 2

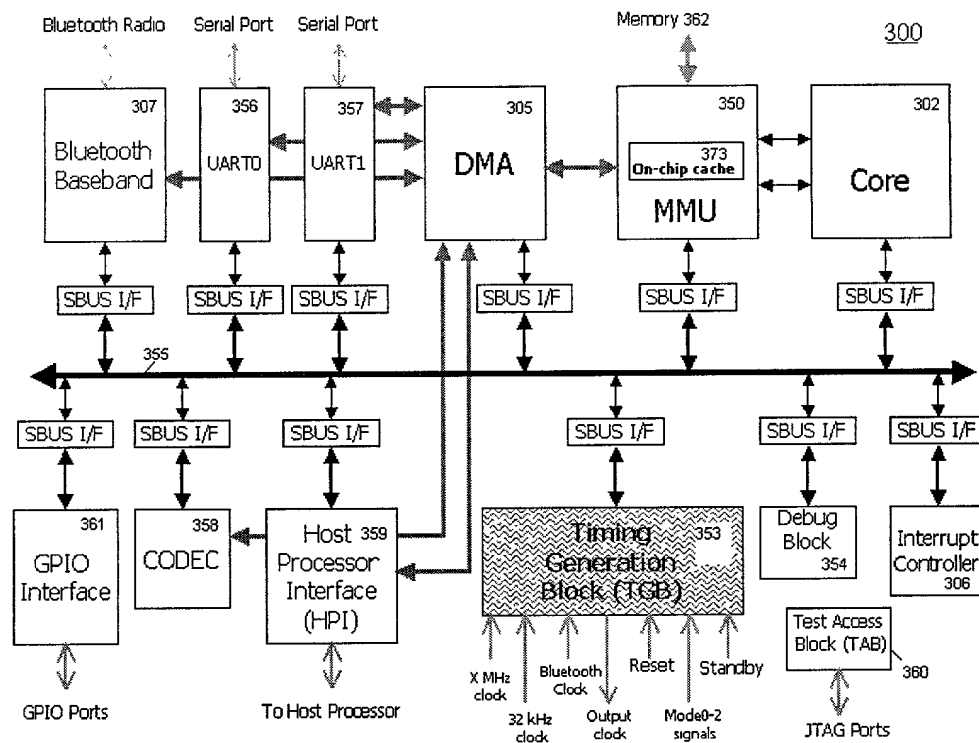


Figure 3a

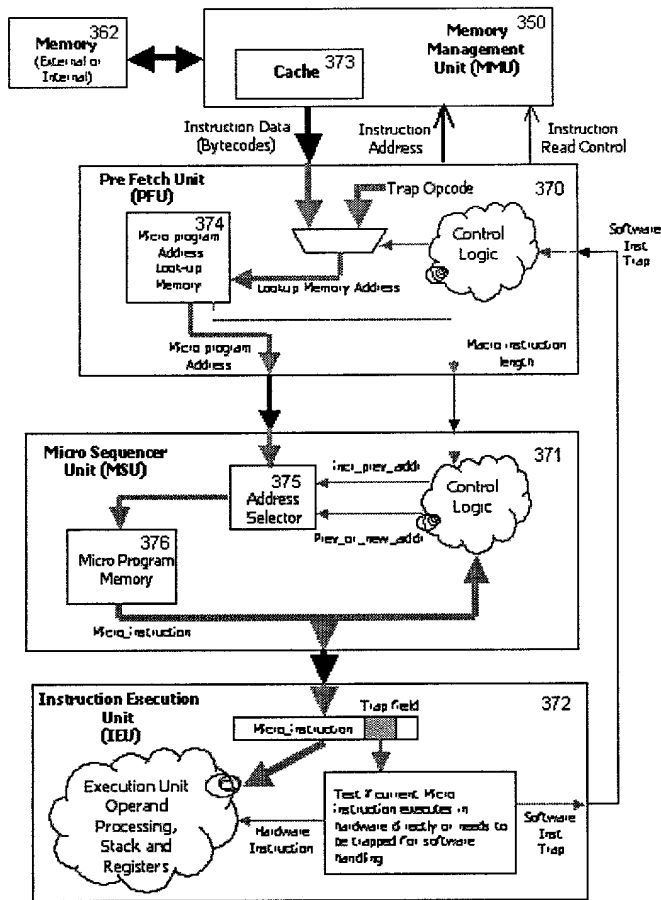


Figure 3b

**Upon a trapped instruction which is not directly executed in hardware:**

- 1) Current Opcode is loaded into a register used to handle vector table bases (in IEU)
- 2) Some registers are swapped
- 3) Some registers are pushed onto the stack
- 4) Software execution transfers via the vector table setting
- 5) Current opcode is translated via software into a sequence of opcodes that can be executed directly in hardware
- 6) This opcode sequence is then executed in place of the current opcode

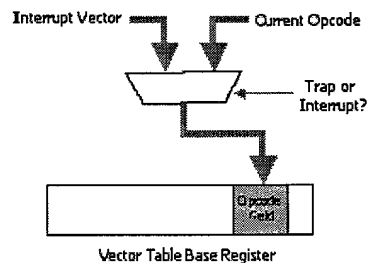


Figure 3c

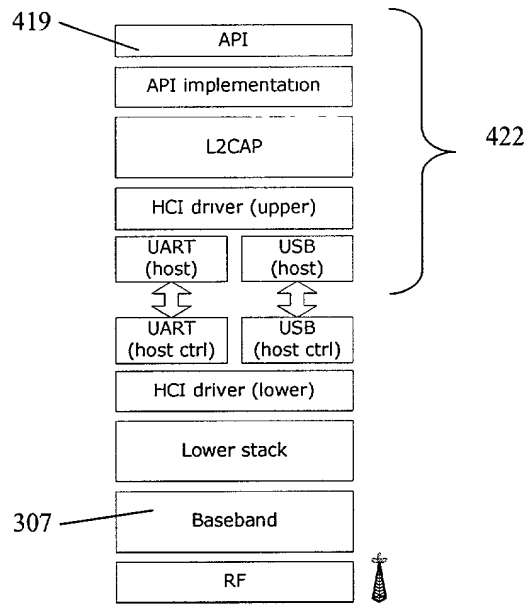
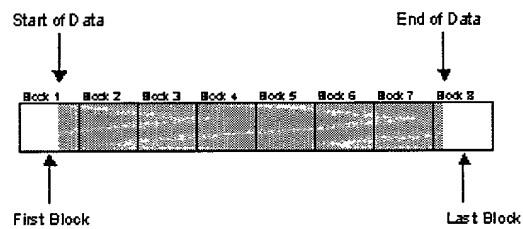
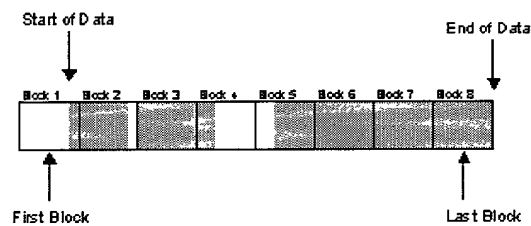


Figure 4

### Figure 5



**Figure 6a**



**Figure 6b**

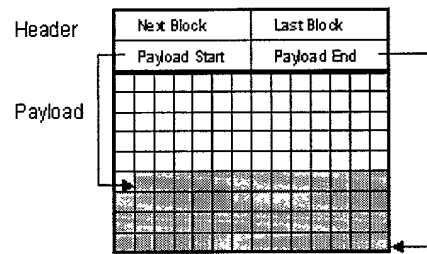


Figure 6c

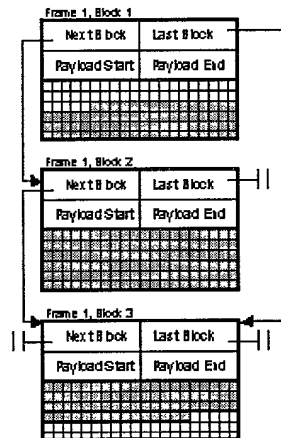


Figure 6d

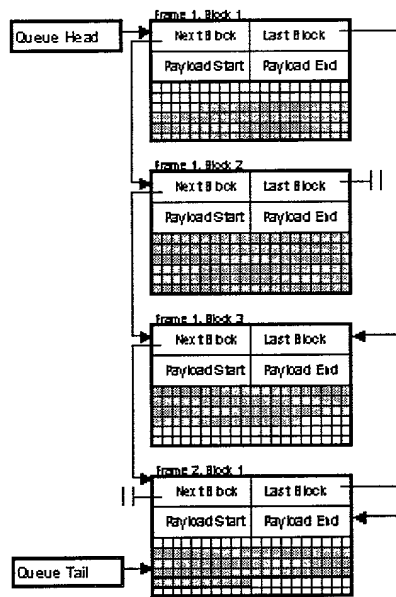


Figure 6e

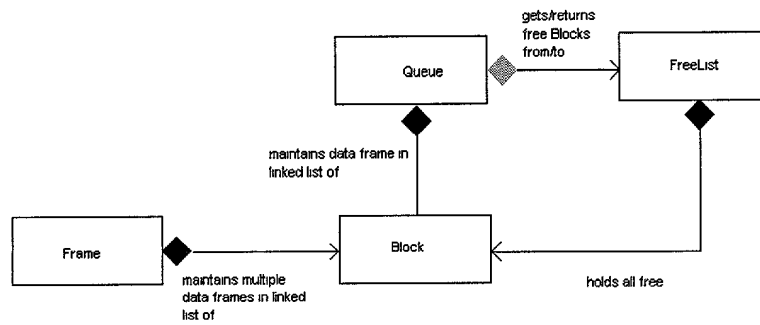


Figure 7a

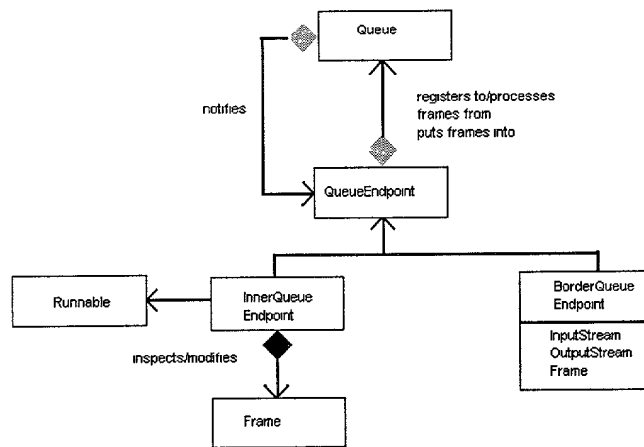


Figure 7b

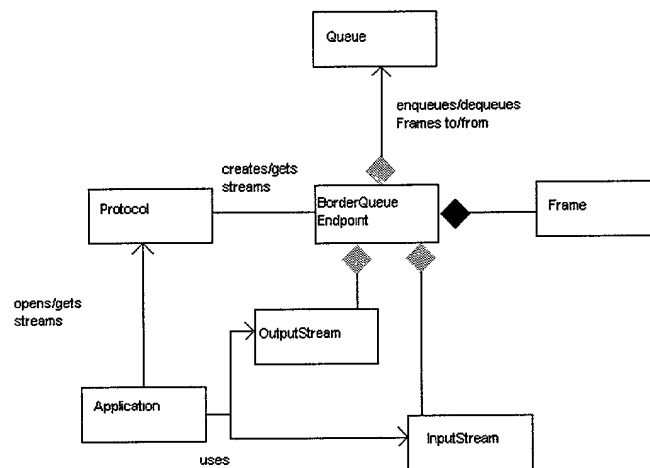


Figure 7c



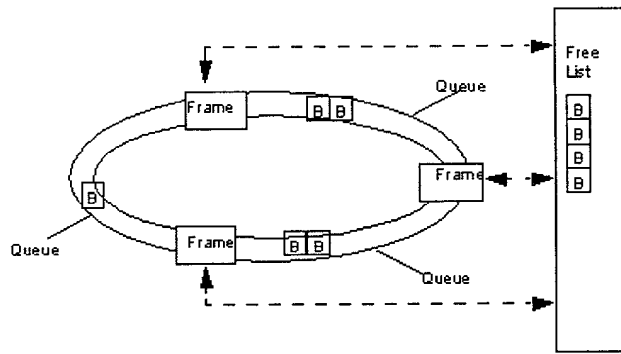


Figure 8

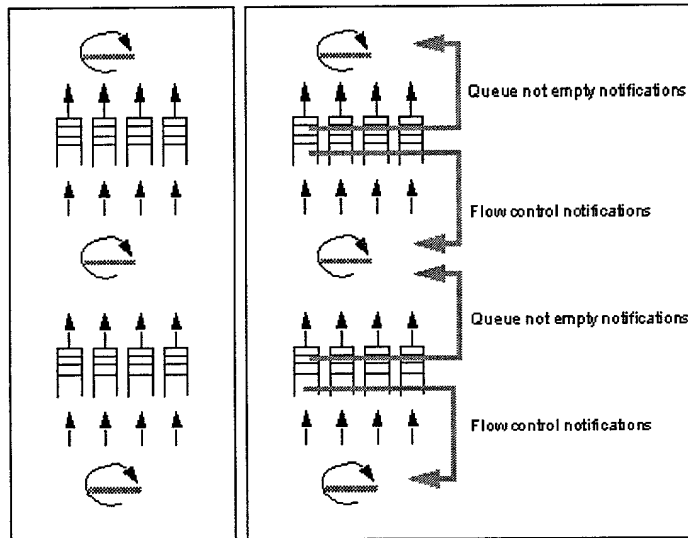


Figure 9



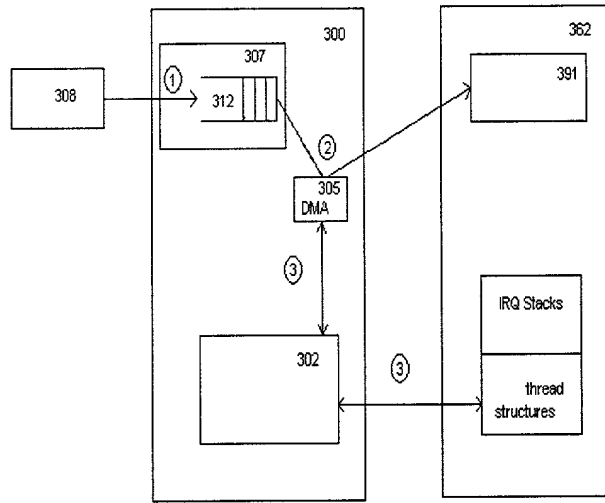


Figure 12

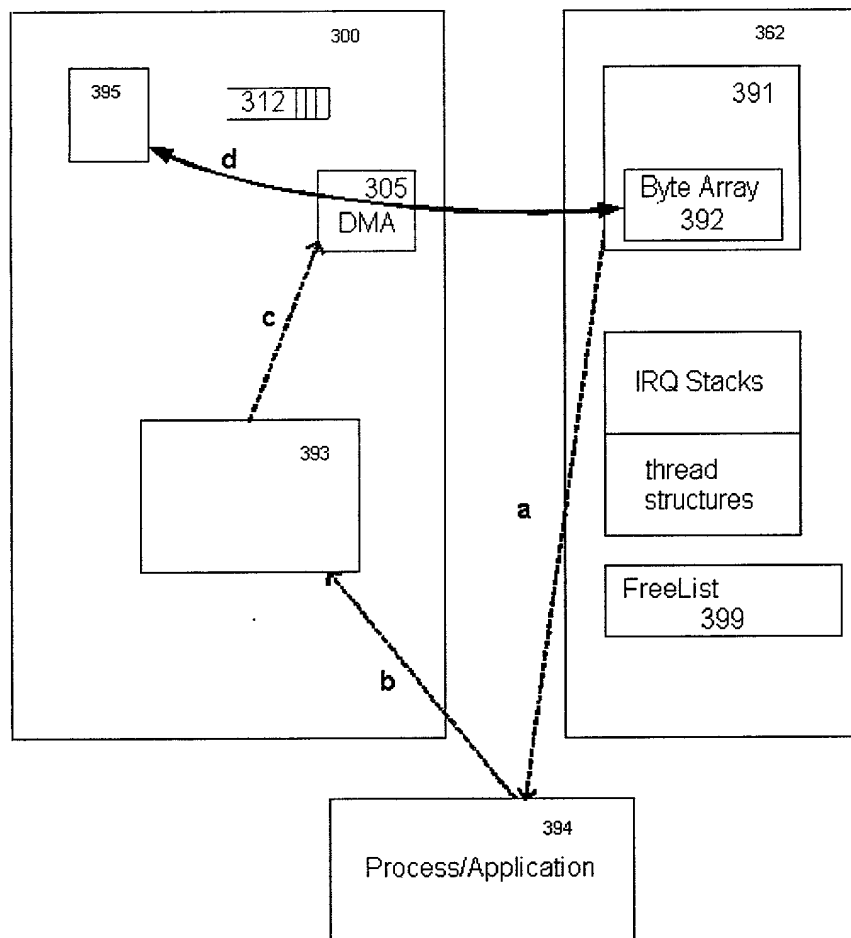


Figure 13